However, as any personal computer (i. e. IBM PC, Atari) provides a V24-interface, at least one interface of this type should be available.
There are several industrial designs for VLSI chips available, which simplify implementation of parallel interfaces. Among them, there are the IEC- and the SCSI bus. The IEC bus normally is used for connection of measuring instruments but requires a specific and very expensive connection cable between the devices. Using a SCSI bus a simple flat cable is needed. Additionally, a component was found that integrates a complete SCSI interface together with DMA drivers in one single chip. In comparison with it, other well-known IEC bus components need external logic and drivers. Accordingly, the SCSI bus was chosen which has counterparts in many computer systems used by radio amateurs.

Design integration

After basic circuit design and test attempts have been made to integrate the complete system on a board with dimensions of 100 x 160 mm (so-called Europe board). The main advantage of this pcb format is that the controller fits into 19" racks. Furthermore, many boxes of these dimensions are available, the pcb of the TNC2 having the same format, for example.
Despite of using highly integrated components integration could only have been realized by solely applying SMD components. However, assembling of the kit should be not only for experts but for hams in the first place, the design was adapted to the room available on the board. Single component groups could be simplified considerably due to exchange of the NEC V50 processor against the software compatible NEC V25. Following the processor exchange diverse digital control logic as well as I/O ports could be saved. Additionally, the new processor provides a second V24 interface and supports multitasking.
At the same time dynamic RAMS were substituted by static ones due to considerably lowering of price and dimensions of static RAMs. Now there was room enough that beneath the real-time clock status LEDs as well as a serial EEPROM could be integrated on the board. Deliberatly, no modem was included in the circuit design because evolution goes on very fast on this sector [2]. All signal lines are attached to a 96 pin indirect connector. The signal lines are arranged in a way allowing direct connection of the SCSI bus via back plane. The modem signals can be lead intersectionfree onto 20 pin flat cable connectors [2]. Additionally, two 8 bit I/O ports for control and measuring purpose are available at the indirect connector.
Because of the exorbitant high component density a two layer pcb could not be used. According to this and to improve EMC behavior, the pcb was carried out with six layers. Against common manner, the power planes were arranged on the outsides of the board to achieve maximum shielding of the routes. Thus, inevitable reciprocal interference between RF and digital components is minimized.

How does FALCon look like ?

After this glance backward on the evolution of FALCon a detailed description of construction and function of the whole design is given. On the pcb, following components are present:

- V25 CPU with a clock rate of 8 or 10 MHz,
- EPROM socket for EPROMs from 2764 to 274000 (8 kB to 5 12 kB),
- two static RAMs with 128 and 5 12 kB capacity, resp. (1 MB together),
- two or four SDLC/HDLC ports with DMA control,
- two V24 ports,
- SCSI controller,
- real-time clock,
- serial EEPROM,
- accumulator or buffer battery for real-time clock and RAMs,
- watchdog circuit,
- external power fail detect,
- twelve LEDs (three per HDLC/SDLC channnel),
- universal 8 bit I/O port,
- 8 bit input port, as well usable as AD converter,
- 96 pin indirect connector with all signal lines attached to.

The 8 MHz version of the the V25 can be used as well as the faster V25+ with 10 MHz clock rate. **The advantage** of V25+ processor is not only the higher clock rate but also the improved DMA block. The processor clock is derived from a quartz oscillator with double frequency. 'This clock rate is independent of the HDLC controller s working frequency which is generated seperatcly. Though, changing the processor frequency **will** not influence the HDLC baud rate. The processor frequency can be lowered software-controlled to reduce power consumption. In comparison with standard processors of the 80XXX series the V25 provides extremely improved abilities to support real-time multitasking. Among these features are for instance eight register banks which can be switched using a simple command. Changing the task, saving of the enviroment and restoring of registers is not necessary. These register banks can also be used for interrupt handling At entry into the interrupt routine the pertinent bank is used and on exit the old status is restored automatically.

Additional features of the processor are: two freely programmable 16 bit timer, a time base generator, an interrupt controller, two DMA channels, an asynchronous serial interface equipped with a baud rate generator, an alternatively synchronous/asynchronous usable serial port with baud rate generator, three 8 bit I/O ports and an analog/digital 8 bit comparator port.

For support of the serial interfaces the V25 provides so-called macro service functions. These functions are equivalent to a micro program controlled DMA, so that the interrupt load is minimized when using the serial ports.

On the pcb, two of the three I/O ports are reserved for internal use and not available for the user. The third I/O port as well as the comparator port are attached to the indirect connector and though externally usable. The I/O port can be configured bitwise as in- or output with software commands. For instance, it can be used to interface the widely spread IIC bus. If required, the count of output lines can be multiplied by use of shift registers and latches. All I/O and comparator lines are equipped with pull-up and pull-down resistors, resp., to protect the CPU and avoid undefined states.

As mentioned before, the four SDLC/HDLC interfaces are realized with special components compatible to the 8530 providing an additional 4 channel DMA driver. During receiving and transmission no interrupts character by character are required. The transfer is handled only by the integrated high speed DMA. An interrupt is triggered only at begin and end of a frame to signal the CPU that action is required. Futhermore, the SDLC/HDLC controllers provide a 10 level deep state FIFO per channel which allows receiving of high speed back-to-back frames. For instance, while the CPU is reacting on the first frame received, data of the second or following frames are transferred to the main memory. Length and status of the first and following frames are held in the FIFO until the information had been processed by the CPU. The four ports can - as known from the SCC 8530 - be used as asynchronous interfaces if more than the two originally present asynchronous ports are needed. Another special feature of the SCC component used here is that all registers can be adressed without an index register. All modem signals are attached to the indirect connector (RTS, CTS, DCD, TxD, RxD, TxC, RxC, DTR and SYNC). Equal to the I/O ports, all input lines are equipped with pull-up and pull-down resistors, resp., to protect the CPU and avoid undefined states. Additional, there are three LEDs including drivers per SDLC/HDLC channel These LEDs are controlled by the signals RTS (PTT), DTR (state) and DCD a.nd though are equivalent to LEDs belonging to a TNC2 system.

The SCSI interface of FALCon is designed for use in high speed networks Data transfer between the main memory and the SCSI bus is carried out using a channel of the internal DMA of the V25. The main part of functions required to control the SCSI bus is hard wired. Furthermore, the component contains all required drivers. If not needed, the SCSI component can be omitted.

Another features are the serial EEPROM, a watchdog circuit and an external power fail input.

The serial EEPROM uses jointly two lines of the 8 bit port. These two lines can be used for diverse tasks, because the select signal for the EEPROM is generated internally and independent of the two lines.

The watchdog circuit is equipped with the well-known component MAX 691.. If an internal port line of the processor is not attended for longer than 1.6 seconds the system will be resetted.

The external power fail input can be used to watch an external power supply. With aid of this facility it is possible to check the unstabilized voltage before passing the voltage regulator. If this voltage descends under a chosen value, the power fail logic sends an non-maskable interrupt (NMI) to the V25 CPU. In this case, a software routine can run several

saving operations before the power supply of the CPU is breaking down. The power fail input has a. trigger threshold of 1.25 V. If a higher voltage is to be watched, it has to be divided by resistors down to 1.25 V.

How to connect FALCon to the outer world ?

The answer on this question is dependent on the application Minimum requirement is a 5 V power connection. A simple 5 V voltage regulator is sufficient for this purpose.
As there are no modems integrated to keep FALCon up to date, modems have to bc connected externally, too. It is possible to use any common modem type. For users a adapter board is available which contains voltage regulators and connections for all interfaces. Both V 24 interfaces are attached to 9 pin DSUB connectors;.. In contrast to to the serial ports, the four modem interfaces are wired to a 20 pin high speed connector as described by Henning, DF9IC [2]. The SCSI interface can be externally connected to a 50 pin flat cable connector. Additionally, there is a litte interface for connection of a LCD display.
For use at net nodes, a back plane is in preparation which provides direct connection of several FALCons through the SCSI bus. On this pcb, there are also flat cable connectors for modems and V 24 interfaces. If needed, the SCSI bus can be active terminated on this board.

Up to now, a WA8DED compatible firmware with hostmode support via the V 24 port was implemented onto the new hardware as well as the newly developped s&ware by Walter, DG9EP, called DigiWare. This program is compatible with the European FlexNet auto-router system, which uses a hop-to-hop procedure with link runtime measurement and other features. A node softvvare compatible to NETROM or THENET has also been implemented.
At the time. of this publication implementation of a hostmode interface via SCSI had already begun. With the aid of the SCSI controller and a small resident program on the host computer the system behaves similar to a common hostmode-TNC - with considerable advantages in speed and comfort for the user. This SCSI hostmodc is especially suited to connect a mailbox system to a FALCon net node.

Interested users and programmers can order a user guide (available only in German). This is a complete documentation of hard- and software containing all technical data and the schematics.

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