Correlation for Direct Sequence Spread Spectrum-The design of a simple data extraction circuit, using serial acquisition in conjunction with a Delay-Lock tracking loop.

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kywords: Direct Sequence Spread Spectrum, Correlation, Acquisition, Delay-Lock Loop, De-spreading.

Introduction

Spread Spectrum systems have become very 'trendy toys' in the areas of radio engineers and enthusiasts. Not only they provide privacy to the user, as an extend the ingenious channel encoding techniques involved make such systems very challenging for communications engineers and radio enthusiasts. Direct Sequence systems are the most preferred as they are the easiest to play with.

Sadly, among the articles and textbooks written on Spread Spectrum there are not many examples provided to the amateur radio enthusiasts. The concepts behind SS applications tend to be rather difficult to grasp and thus put the radio enthusiast in a very difficult position in terms of understanding and designing of such a system.

As an extend, some already available examples demand the use of complicated circuitry and expensive ICs. Thus, *amateur radio enthusiasts are put in the risk of loosing valuable time and money in case of failure or possible damage of expensive components due to the idiosyncrasies of such ICs. Thus an easy and cheap solution is necessary.

This article is written in order to explain the concept of correlation in the simplest possible way to the amateur radio enthusiast and thus provide a simple solution concerning the heart of the system, i.e. the circuit that performs the de-spreading. It could be used as reference or a manual and the circuit described has the potential to be adjusted to any Direct Sequence SS system used for digital data transmition.

Demodulation and de-spreading for DS SS systems

At this early stage, the best way to understand correlation strictly speaking in terms of DS is to visualise the DS SS signal as a digital data stream with two types of modulation imposed onto it. At the transmitting side the following two actions are necessary.

- Spreading modulation, which 'spreads' the digital signal. It is used for channel coding purposes.
- RF modulation, which is the conventional part of modulation used for transmition.

Consequently at the receiving side of the system the exact opposite actions will have to be taken, in order to recover the data.

- RF demodulation, which ‘cleans up’ the spread signal from the radio frequency used for transmition. What is left after this action is the digital data stream ‘carrying’ the spreading code onto it.
* Demodulation of the spreading code. This is by far the trickiest part of the task and it is the ultimate recovery stage of the receiving system. It gives back the spread or ‘hidden’ data stream for the next stages of digital signal processing.

This article is solely concerned with the second stage of demodulation described above for DS SS systems. It is assumed that a spreading code cycle is used for each data bit.

This is exactly where the concept of **correlation** jumps in. The receiver must generate a replica of the exact same code used at the transmitter and modulo-2 add it (which is an equivalent mathematical operation to the XOR logic operation) with the received code signal. At this stage the received code signal is the code itself, either inverted or not corresponding to data bits ‘1’ or ‘0’ being received respectively. This is shown below, in Figure 1. [l]

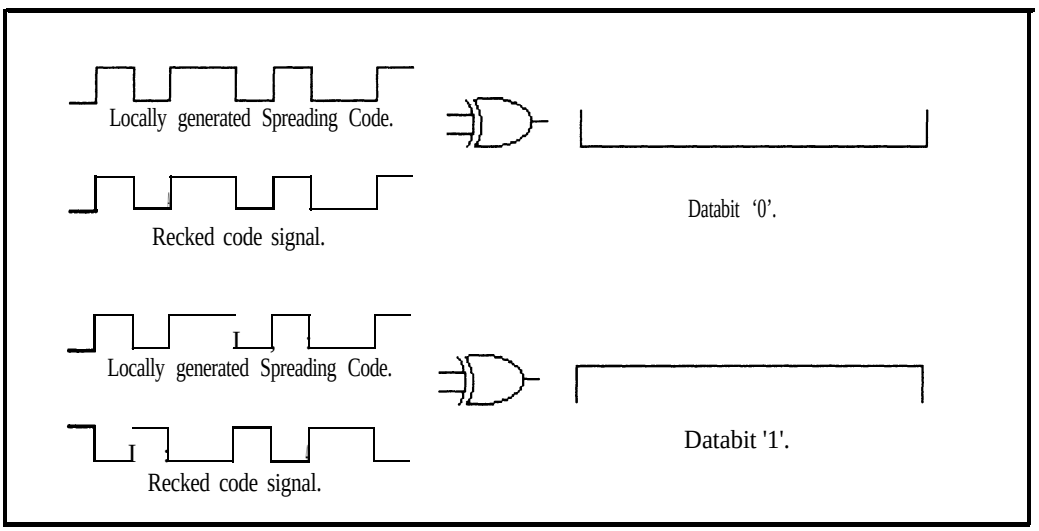


Figure 1 - Data De-Spreading in DS SS

Correlation versus time offset effects

A definition for correlation in DS SS should be given initially: “Correlation is the fundamental process for DS SS systems and is the action of measuring the similarity of the locally generated code, with the received code signal.” The aim of this action as explained above is the completion of the digital data recovery.

In the previous paragraph it was assumed that the locally generated code and the received code signal were perfectly time-aligned. This case slightly departs from what the engineer will face in reality.
Due to uncertainties in the distance between the transmitter and the receiver, which may vary depending on how far the user may want to transmit or how far can the system transmit, propagation delays are caused. In addition to this, relative clock instabilities between the transmitter and the receiver spreading code generators will result into phase differences between the locally generated code and the received

code signal. Note that it is assumed that the receiver and the transmitter spreading code generators are not synchronised with eachother.

Thus, it is almost a certainty that when the signal will be received the locally generated code and the received code signal will not be in perfect time alignment. This is illustrated below in Figure 2. At a random time instant the locally generated code and the received code signal are modulo-2 added, i.e. XORed. Data cannot be recovered, as the two correlated signals are not time aligned.

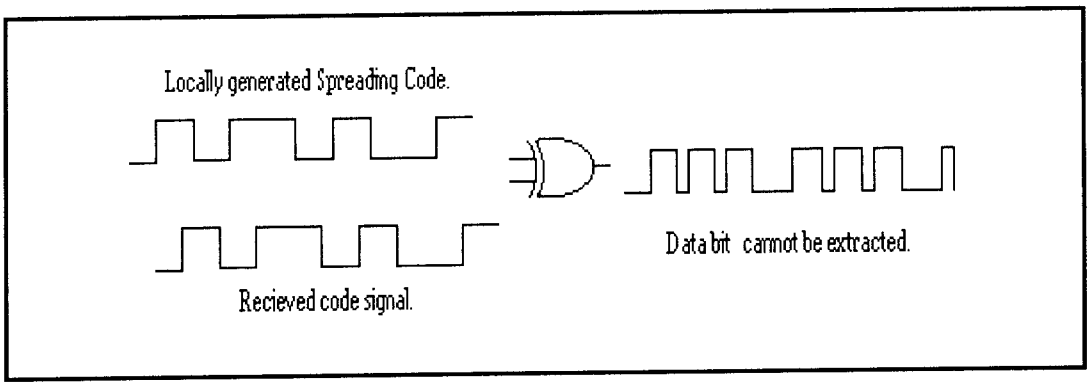


Figure 2 - Despreading without the locally generated code being time aligned with the received code signal.

Mathematically, considering the locally generated code as a time varying function *f(t)* and the received code signal as *g(t)*, correlation is defined with the integral below:

$$\psi(t) = \int_{-\infty}^{+\infty} f(t)g(t)dt$$

Consider the case were a data bit '0' was transmitted. This effectively means that a non-inverted code cycle was received. The receiver will now have to time align the received code with the locally generated code. Thus mathematically the received code signal can now be re-expressed as a time shifted version of the spreading code. Therefore: $g(t)=f(t-\tau)$, and the correlation integral can be expressed as:

$$\psi(t) = \int_{-\infty}^{+\infty} f(t)f(t-\tau)dt$$

where τ is the time shift

This is the auto-correlation integral. Due to the properties of a well behaved maximal length code like the one that was used for the circuit described later, the correlation integral gives the triangle function as presented below in Figure 3.

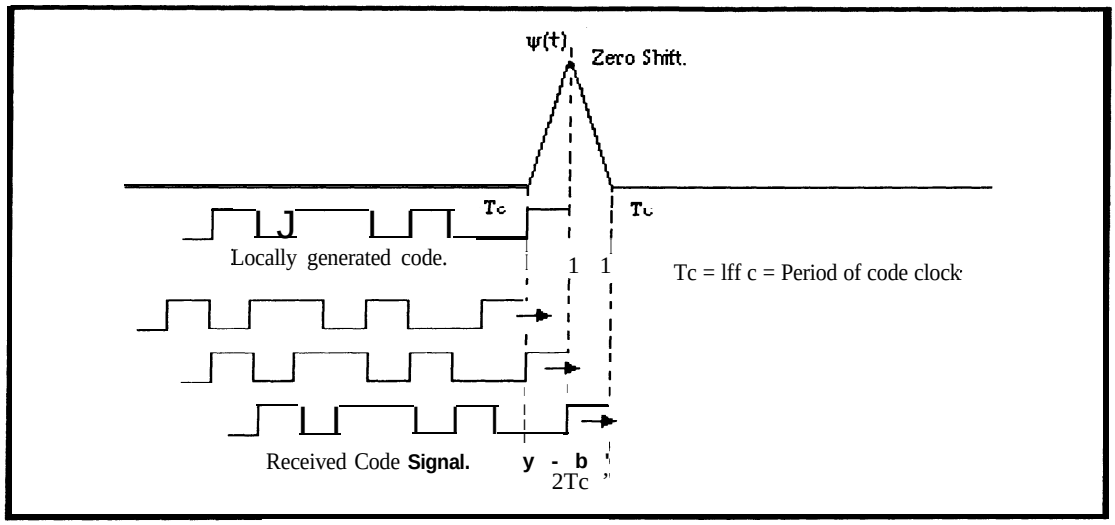


Figure 3 - The autocorrelation function of a maximal length code

The generation of this resulting triangle can be visualised by imagining the received code signal sliding past the locally generated code in search for perfect time alignment. In terms of mathematics the integral simply symbolises the area generated under the product of the received code signal and the locally generated code as one slides past the other. Due to the properties of maximal length codes any product out of the region where the two correlated signals are one chip apart will be negligible compared with the products within the time region of one chip separation. Maximum output occurs for zero time shift, i.e. for z=O, or otherwise perfect time alignment.

The use of maximal length codes is strongly recommended as their correlation integral produces a single triangle making de-spreading an easier task.

If a data bit '1' was transmitted then the case is quite similar except for the fact that the correlation triangle would appear with 'pointing' downwards. [l]

Acquisition

This section deals with the ideas and considerations of how to bring the locally generated code and the received code signal into perfect time-alignment. This process is known as acquisition.

The device designed to perform acquisition must be able to produce a voltage output proportional to the similarity between the two correlated signals. This voltage then, will have to be compared with a threshold, set to statistically decide whether the two signals are perfectly time aligned or not. If they are not perfectly time aligned, the acquisition circuit must then decide to perform a systematic search through the time and phase uncertainty region between the two signals and thus find the exact time instant when the two signals are perfectly time aligned.

Acquisition can be performed serially or in parallel. The cheapest solution is provided by a serial search, which is the technique used for the circuit that will be described later. [I]

The frequency uncertainty problem

Suppose that perfect time-alignment, between the locally generated code and the received code signal has been accomplished. One could say it is obvious that data could be extracted from that point. This is not the real case.

Due to minimal, but not negligible relative frequency offsets between the receiver's clock and the transmitter's clock the received code signal will arrive at a slight different frequency compared to the locally generated code. As a consequence, when synchronisation has been achieved the two signals will try to drift apart from each other resulting loss of synchronisation. Again, it is assumed that the receiver's and the transmitter's code generators are not synchronised with respect to each other.

This is another problem that the designer must overcome. It is of major importance to maintain synchronisation. The idea is to force the receiver's code clock to run at the same frequency as the received code signal. This is achieved by means of feedback loops and the process is called tracking.

Tracking is used in conjunction with acquisition must be initiated right after synchronisation has been achieved. [l]

Tracking methods

The two methods used are the delay lock loop and the tau dither loop. The delay lock loop is presented in Figure 4 below. The received code signal is split into three different channels and is mixed with three replicas of the spreading code. Two of the replicas have the same time offset with respect to the third. One is advanced by a fraction of one chip time duration and the other is retarded by the same fraction of one chip time duration.

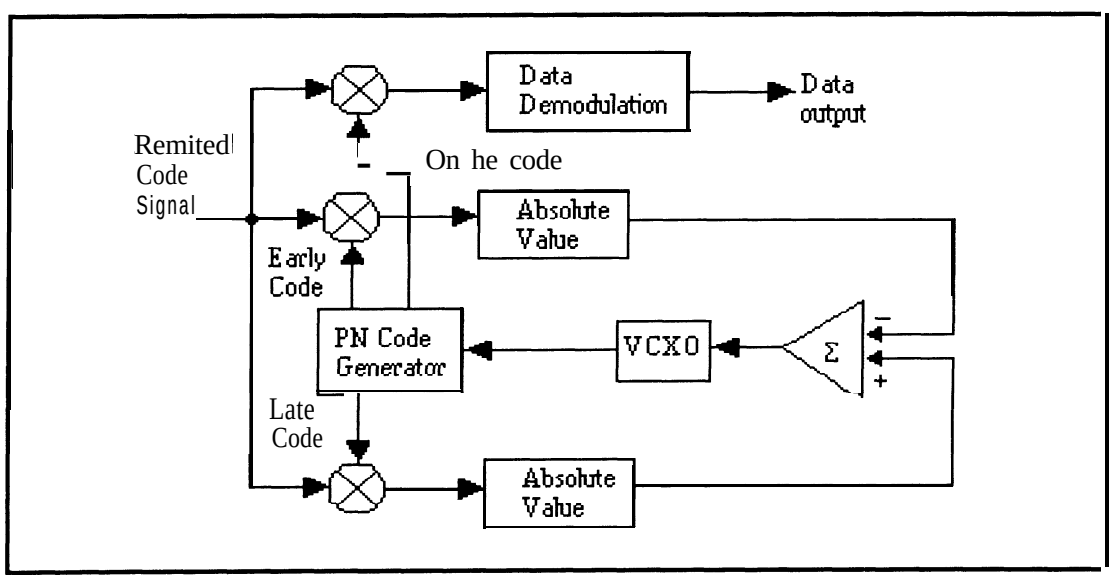


Figure 4 - The Delay Lock loop for DS spread spectrum signals

These two replicas are used for the delay lock loop whereas the third is used at a separate channel to perform acquisition. Thus the names 'early' and 'late', with respect to the 'on-time' code. Due to the

fact that both of the codes have the same time offset with respect to the on-time channel, when perfect time alignment is achieved at the on-time channel, their mixing stage outputs are made equal with the aid of absolute value circuits independent of whether a data bit ‘1’ or ‘0’ was recovered. Thus solely the degree of matching is converted to DC levels.

As the received code signal and the locally generated code tend to drift apart from each other, the absolute value outputs will differ. Their difference is used to steer the voltage control crystal oscillator (VCXO) that drives the code generator. Thus the locally generated code can be forced to catch up in frequency with the received code signal. Consequently perfect time alignment between the locally generated code and the received code signal is maintained and data can be continuously extracted.

The tau dither loop does not provide the engineer with the same flexibility in terms of steering as the delay lock loop and will not be examined. [l]

The de-spreading circuit’s block diagram

This circuit was designed for a DS SS system with a digital data stream at 9600 kbps. A maximal length code of 255 chips was used.

The received code signal is split into three channels, one performing serial sliding acquisition and data extraction, while the other two are used for the delay lock loop as presented in Figure 5.

In an earlier part of this report the de-spreading concept was explained with the aid of XOR gates for simplicity. Double balanced mixers substitute the XOR gates for this application. The double balanced mixers are configured in such a way to give output voltage amplitudes corresponding to the degree of matching between the received code signal and the locally generated code.

It is recommended that, the two code replicas used for tracking, should be separated by a half chip with respect to the on-time code. This will be explained in the next paragraph. For this particular application the codes were stored in an EPROM (Erasable Programmable Read Only Memory).

Initially the VCXO is switched to a certain input tuning voltage and hence the locally generated code is clocked at a smaller frequency compared to the clock frequency of the transmitter. This effectively provides serial sliding acquisition. Thus the locally generated code will ‘see’ the received code signal slide past it, at a relatively higher frequency. Thus, a scan through the total time and phase uncertainty region is achieved until the two signals are perfectly time aligned.

At the acquisition channel, two outputs were taken from the DBM. One is used for data extraction whereas the other is used to indicate, whether synchronisation has been achieved or not and thus turn the delay lock loop on.

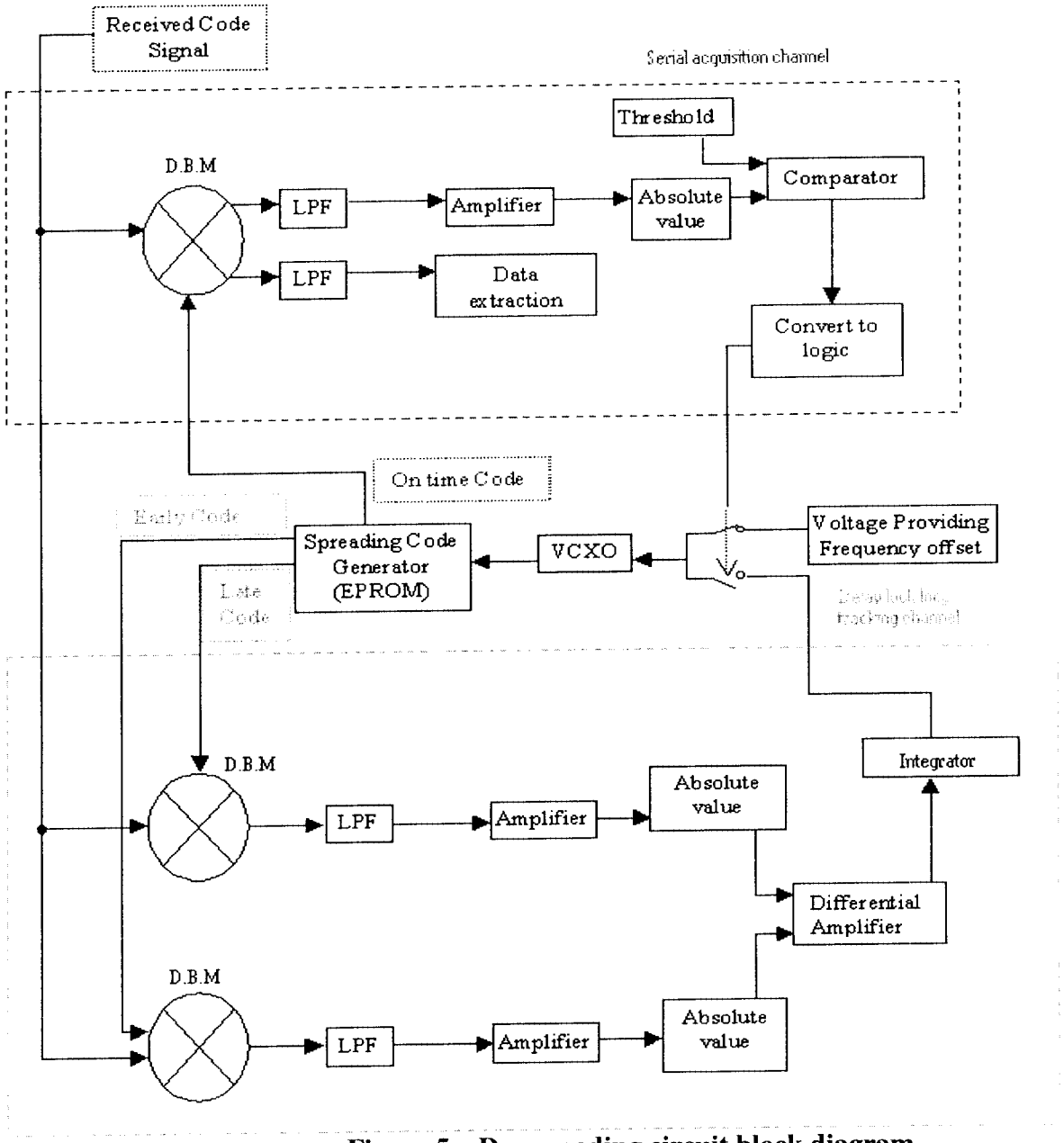


Figure 5 – De-spreading circuit block diagram

Both of the outputs of the DBM are low pass filtered to get rid of the unwanted noise delivered to the de-spreading circuit together with the received code signal after the RF demodulation stage. The second output after low pass filtering is amplified in order to provide larger voltage levels corresponding to the degree of matching. Here, the aim is to provide a dc indication corresponding to how well the two signals are time aligned with respect to each other.

The output of the DBM used to provide an indication whether synchronisation has been achieved or not, gives its highest possible output voltage value when the locally generated code is perfectly time aligned with the received code signal being the code inverted corresponding to a data bit '1' transmitted. The lowest possible voltage value is output when the locally generated code is synchronised with the received code signal being the code non-inverted corresponding to data bits '0' transmitted.

Consequently two different voltage levels correspond to the same degree of matching between the locally generated code and the received code signal. The circuit has to be able to identify both of these cases as the same in order to provide an indication whether synchronisation has been achieved or not, independent of the bit that was initially transmitted. Thus an absolute value circuit is used, and for both of the cases described above the same voltage levels were output, corresponding to the same degree of matching, independent of the transmitted bit.

This voltage level is then compared with a threshold voltage in order to provide an indication whether synchronisation has been achieved or not. At the time instant where synchronisation was achieved the threshold was exceeded and the output of the comparator switched to is maximum. The output of the comparator is then converted to logic levels and hence when synchronisation is achieved the tuning voltage of the VCXO, is switched from the one that was providing the frequency offset resulting to sliding acquisition, to the output of the delay lock loop. The VCXO is tuned to run at the same frequency of the transmitters code generator frequency when no error signal is delivered from the delay lock loop. By this switching operation the delay lock loop's operation is initiated.

The exact same tactics are used at the other two channels, the early and late channel, in terms of mixing the two signals and the conversion of the degree of matching to voltage levels. Thus low pass filtering, amplification and absolute value circuits are used for the reasons explained above.

To maintain synchronisation the outputs of the absolute value circuits are summed in a difference amplifier and their difference generates an error voltage with the aid of an integrator to steer the VCXO, forcing it to catch up with the received code's frequency. The integrator's output is proportional to the integral of the output of the difference amplifier, resulting frequency changes to the VCXO proportional to the rate the two signals are drifting apart from each other. Thus continuous data extraction is achieved. [l]

Half chip separation of the early and late with respect to the on time code

This part presents a simple explanation why a half chip separation should be preferred for the late and early spreading codes with respect to the on time code. Note that here the XOR de-spreading concept is employed again. Figure 6.

Suppose that the received code signal and the locally generated code are synchronised. At this certain time instant due to the half chip separation, the outputs of the XOR gates at the early and late channel are exactly the same. If they are both integrated, then the outputs of the integrators will be voltage levels proportional to the areas under the outputs of the XOR gates. (i.e. the integral of the XOR outputs.)

Supposing that at this time instant the locally generated code is driven by the VCXO at a higher frequency compared to the frequency of the received code. The outputs of the XOR gates will differ as presented in Figure 6.

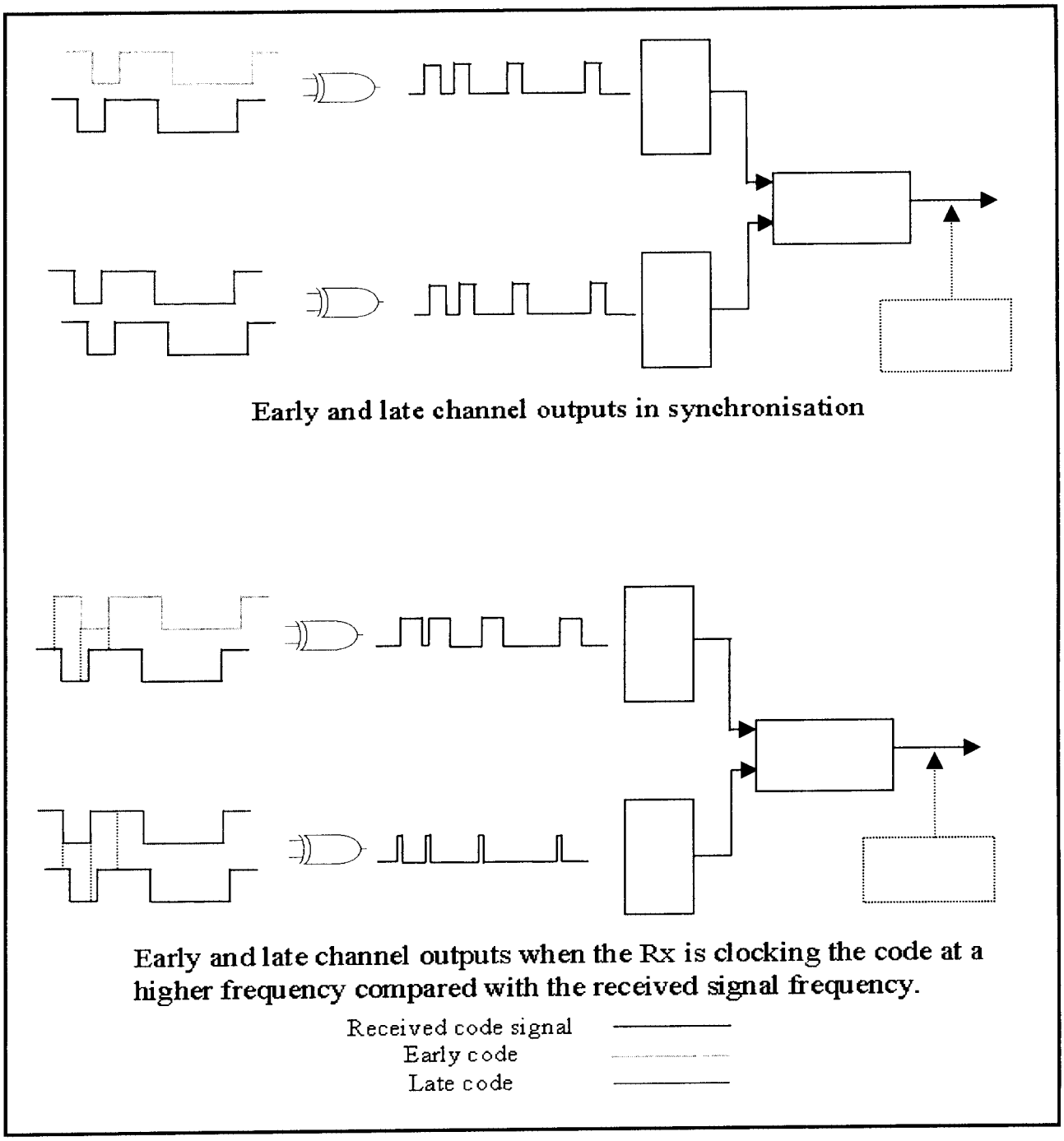


Figure 6 – The effect of a half chip separation between the early and late codes with respect to the on time code as the two signals drift apart from each other.

As a result the integrators will deliver different voltages at their outputs, as the area under the outputs of the XOR gates is different.

But it is the rate of change between the outputs of the integrators, which causes the VCXO to catch up with the received code signal's frequency. The smaller the time distance between the early and late

codes with respect to the on-time code the larger the rate of change at the output of the difference amplifier. [I]

Detailed analysis of the de-spreading circuit

MC1496 active DBMs were used. An alternative version of the product detector (refer to MC1496 datasheet) circuit was used, and is presented in Figure 7. Both of the on-time channel DBM outputs were used (Ul). The 47kQ pot's wiper must be centered to eliminate the presence of the spreading code on top of the data stream, when the two signals are synchronised. At pin 6, when the locally generated code was synchronised with the received code non-inverted the output was at 6.4V. For synchronisation with the received code being inverted the output was at 9.W. Pin 12 was the complement of pin 6.

Both of the outputs where then low pass filtered by first order RC filters. The output from pin 6 was then scaled by a 2.2V zener diode down from 4.2V up to 7.6V for synchronisation achieved between the locally generated code and a non-inverted or inverted received code respectively. After low pass filtering an amplifier was used (U4) with one input referred to ground and the second to a voltage divider giving not only the ability to amplify the signal but also to set a 5V mid-line between the maximum and minimum outputs which were from 2V up to 8V. This trick gave the ability to the full wave rectifier (U5&U6, i.e. the absolute value circuit) to output voltages corresponding solely to the degree of matching between the two signals. Thus the output of the rectifier was made indeperxient, whether a data bits '0' or '1' where de-spread. The output of the rectifier was from 5V to 8V.

After low pass filtering again the rectified signal was compared with a fixed threshold voltage at approximately 6.5V halfway between 5V and 8V (U7). Due to the nature of the code used for this system the degree of matching is always minimal for every shift position except for the region were the correlation triangle is generated. This is mainly the reason why a well-behaved maximal length code should be used. Thus the voltage amplitude at the output of the rectifier was always very small (about 5.1V) and the largest possible (about SV) was rapidly output when the two signals where perfectly time aligned. Thus a threshold decision at 6.5V was a good one. The output of the comparator (U7) was from l.SV to 8SV, indicating synchronisation at 8.5V.

This output was then scaled down from 1.W to 4.6V by a regulator, which is effectively a resistor connected with a 3.9V zener diode to ground. These voltage levels were then converted to logic with Schmitt trigger inverters twice. The first Schmitt trigger inverter (U17) gave a high output while the circuit was trying to acquire the signal and a low output when synchronisation was achieved. The other Schmitt trigger inverter (U19) gave the opposite voltage levels under the same conditions.

Pin 12 output of the DBM was used for data extraction. After low pass filtering again the output was compared with a fixed voltage set at 8.lV, right at the middle between the minimum and maximum output voltages. The output of the comparator (U8) was scaled down and regulated as above, converted to logic using a Schmitt trigger inverter (U18) and low pass filtered.

This inverter's (U18) output, was effectively the data when the locally generated code was synchronised with the received code. The output of the second inverter (U19) described above was then input to an AND gate (U21) together with the data. By this action the data was passed to the audio side of the system only when synchronisation was achieved.

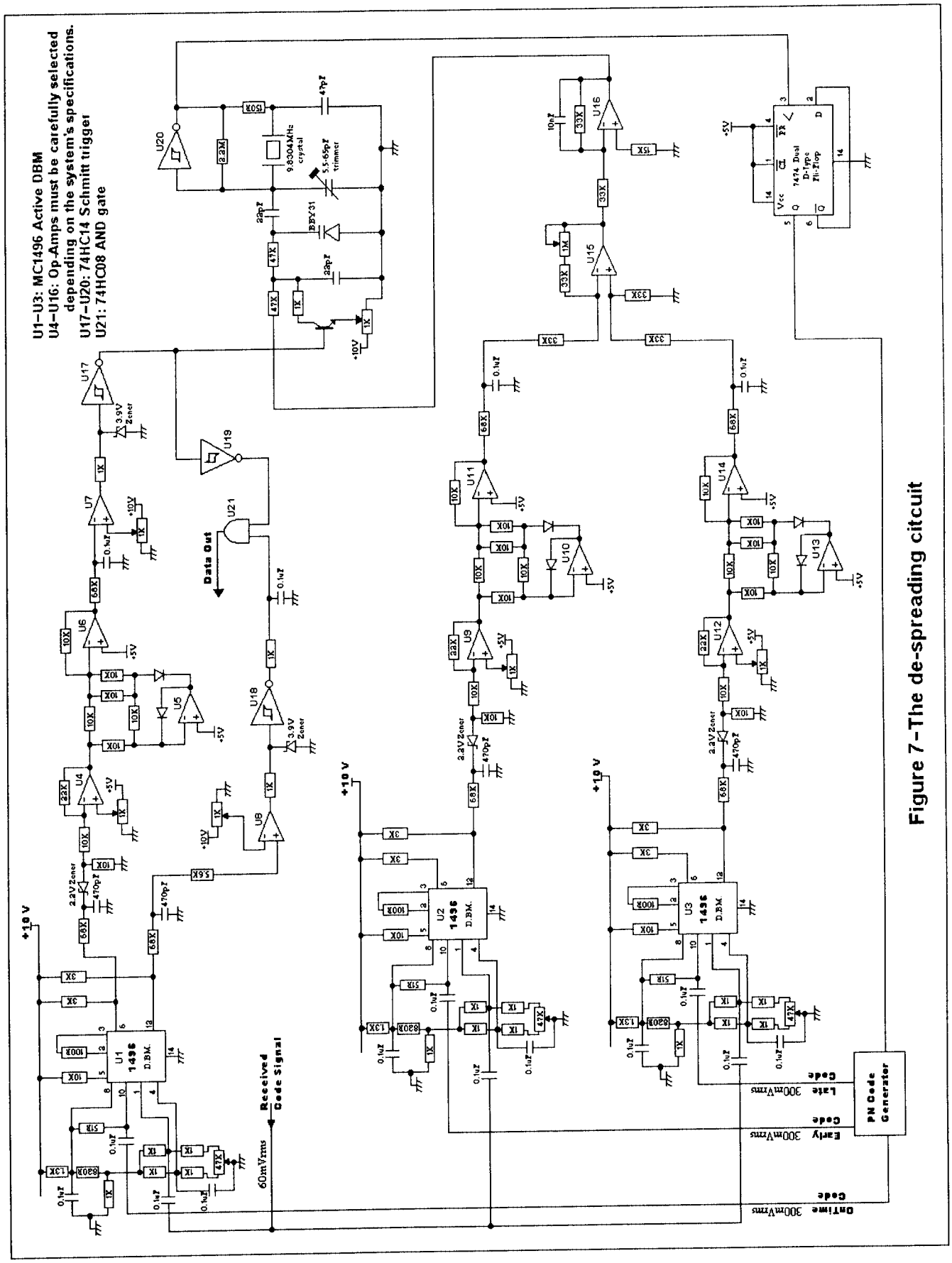
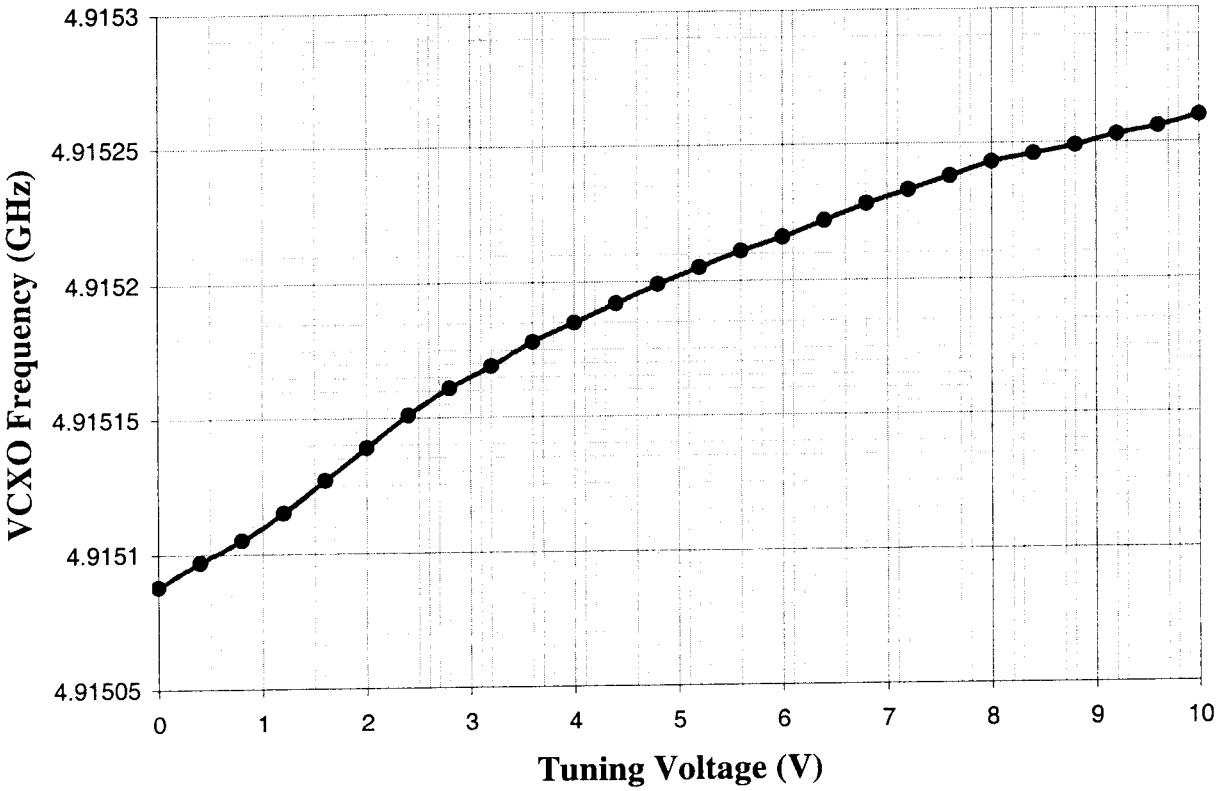


Figure 7–The de-spreading citcuit

For this particular application a 9.8304MHz crystal was used at theVCXO. The frequency of the VCXO was divided by two using a D-type flip-flop. By slowly adjusting the trimmer capacitor, the output of the flip-flop was tuned at 4.9152 MHz, which was the transmitter's code generator frequency, for 5V input tuning voltage. A 5V voltage corresponds to no error voltage delivered to the VCXO by the delay lock loop. See Graph 1.



Graph 1 - The VCXO frequency vs. the tuning voltage (after the /2 stage)

The VCXO was initially given a slight frequency offset providing the sliding of the received code against the receiver's locally generated code. This was achieved by pulling the tuning voltage of the VCXO down to 2.4V by using the first inverter's output (U17) to turn the transistor on. This frequency offset, of about 50Hz, provided the ability to the circuit to slide a complete cycle of the received code against the locally generated code at approximately 4 seconds. Thus the maximum time, to run a complete scan through the total time uncertainty region time, perfectly time align the two signals and thus extract the data was about 4 seconds.

When synchronisation was achieved, the inverter's output was turned down to 0V and thus the transistor switched off. Hence the VCXO tuning voltage was then fed by the delay lock loop. This is effectively how the circuit switched from acquisition to tracking mode.

The same DBMs amplifiers and rectifiers were used for the early and late channels. Both of the outputs of the full wave rectifiers of the late and early channel are passed into a difference amplifier (U16) and an integrator (U18). At the difference amplifier a 1MΩ variable resistor in series with a 33KΩ resistor

was used in order to vary the amplifier's gain. Consequently, the rate of change of the error voltage was made variable. Thus the VCXO was forced to catch up with the received code signal's frequency at a faster rate and stability of the delay lock loop was improved.

This could be used as an example. Any crystal could be used and the frequency offset can be easily adjusted by playing with the trimmer capacitor. Filtering may also change depending on the application. [II

Results and recommendations

The circuit was able to re-construct the data. Exhaustive tests where carried out with the circuit's early late and on time channels constructed on printed circuit board while the VCXO and the code generator were still on breadboards. Initially the circuit did manage to lock and extract the data even with 60dBs of attenuation. In order to test the circuit's ability to recover data under the worst signal conditions the attenuation was set to exceed 60dB and the LNB was set not facing the transmitter. The circuit did not manage to extract data under those conditions.

In reality, for a DS spread spectrum system that is to be tested in environmental conditions, this would turn out to be a problem that must be overcome.

In terms of circuitry the first and obvious thing to do is to use improved low pass filtering at the outputs of the DBMs. A filter with a sharper 3dB frequency is required. Thus it would be wiser to use an active low pass filter of a higher order. Active low pass filters use op-amps and thus the designer should take the frequency response of the op-amp itself into account. As a solution a 'Sallen and Key' second order low pass filter is shown below with a 3dB frequency of around 4.65OkHz (Corresponding to 9.7kbps). It is assumed that the 3dB frequency is in the frequency range of the op-amp. Higher order filters can be used, providing sharper 3dB frequencies but a second order filter should be enough. The capacitor's and resistor values should be selected depending on the application.

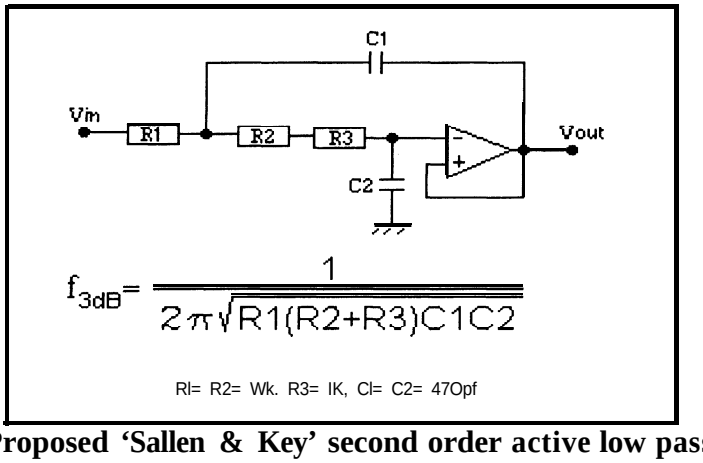


Figure 8 - Proposed 'Sallen & Key' second order active low pass filter

As a second priority, a smaller acquisition time must be provided. The acquisition time of the circuit presented in Figure 7 was about 4 seconds. This is a problem when the user is' trying to align the receiver with the transmitter for ling of sight transmition. Thus rapid acquisition is essential. In order to achieve this, a larger frequency offset should be provided. But first it must be ensured that the frequency offset is within the delay lock loop's capture range. For the circuit configuration presented in Figure 7, the 50Hz

frequency offset was the maximum within the loop's capture range and it was worked out using a trial and error approach.

By substituting the 22pF capacitor between the 470kQ resistor and the 9.8304MHz crystal, with a larger capacitor the VCXO's frequency deviation for a range of tuning voltages from OV to 1OV will be larger. For the 22pF capacitor the frequency deviation was about 175Hz. It was found that for a 33pF capacitor the deviation was 225Hz and for a 56pF capacitor 260Hz. For every capacitor used it was ensured that a tuning voltage of 5V corresponded to about 4.9152MHz. (i.e. the transmitter code generator's frequency). This was accomplished by adjusting the 5.5-65pF trimmer capacitor.

In order to keep the desired frequency offset within the loop's capture range, the time constant of the 1kSZ resistor and 22pF capacitor RC circuit, connected from the collector of the transistor to ground, must be made smaller. By reducing the time constant of the RC circuit the VCXO will switch from its acquisition mode to tracking mode faster. Thus by trial and error again the right resistor and capacitor values can be worked out and consequently the acquisition time can be minimised.

With the current circuit configuration, when the transmitted signal is corrupted, or lost for a short time period, the circuit will switch back to acquisition mode from tracking mode until the data is de-spread again. Extra circuitry could be added in order to keep the circuit on tracking mode for a short time period, before switching back to acquisition mode when the signal is lost. Thus if the lost signal appears again within this time period the circuit will not have to try and de-spread the data again. Such an idea will involve complicated circuitry and it may not be necessary if the acquisition time was made quite small (i.e. a fraction of a second). When the signal is lost, the circuit may switch back to acquisition mode, but when the signal appears at the receiver again the acquisition time will be quite small and data will be extracted again rapidly. [I]

References

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Recommended Reading

1 **SOLAR** B.: **'Digital Communications: Fundamentals and Applications',** (Prentice Hall, 1988) pp. 561-570
Comments: A great introduction.

2 DIXON, R. **C.: 'Spread Spectrum Systems',** (Wiley-Interscience, June 1984), pp. 120-260
Comments: This is a 'must read' book on Spread Spectrum.

3 **'The ARRL Spread Spectrum Sourcebook',** (American Radio Relay League Inc, 1997), Chap. 8
Comments: This is the kind of book I was praying to get my hands on. It helped me a great deal. It covers everything one needs to know on Spread Spectrum. Practical solutions and examples are provided.

4 AGARD (Advisory Group for Aerospace Research and Development): **'AGARD lecture Series No. 58 on Spread Spectrum Communications',** (NATO, 1973), Chaps. 4-5
Comments: This is a tough one. All aspects are explained in the greatest possible theoretical detail. Be very patient while reading this one and take notes.

5 DIXON, R. **C.: 'Spread Spectrum Techniques',** (IEEE Press, 1976), Part V
Comments: A good theoretical reference. Presents articles written on Spread Spectrum.

6 COOPER R. G., McGILLEN C. D.: **'Modern Communications and Spread Spectrum',** (McGraw-Hill, 1986), pp. 296-356
Comments: Another 'must read' book.

7 MAZDA F. F.: **'Electronics Engineer's reference book',** (Butterworths, 5'h edition), pp. '39/12-14'
Comments: Good solutions for circuit design and construction. All the considerations that can be easily forgotten are there.