Design of the TangerineSDR Clock Module

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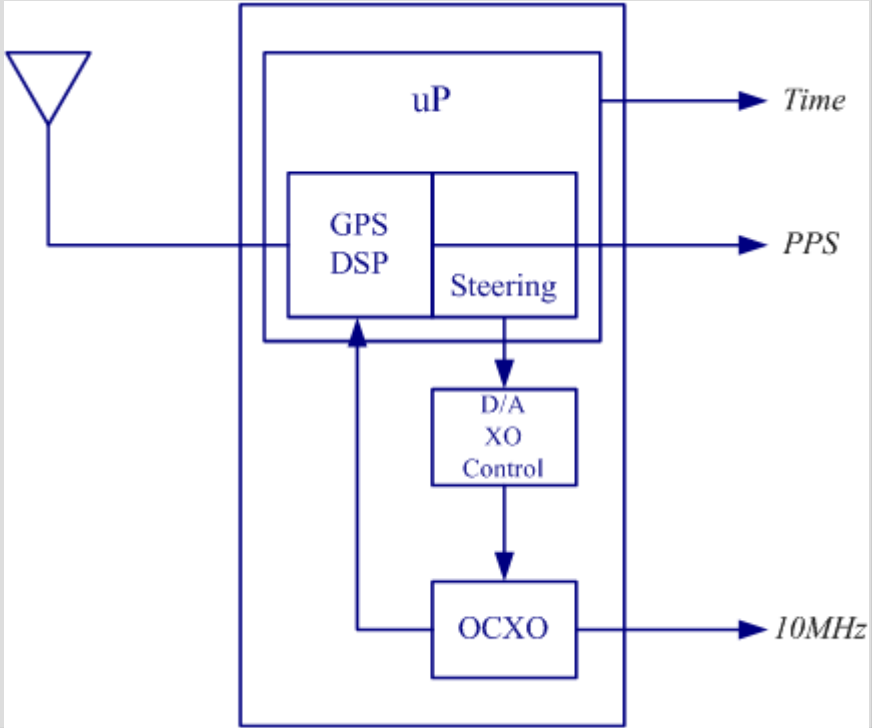
TangerineSDR
Clock Requirements

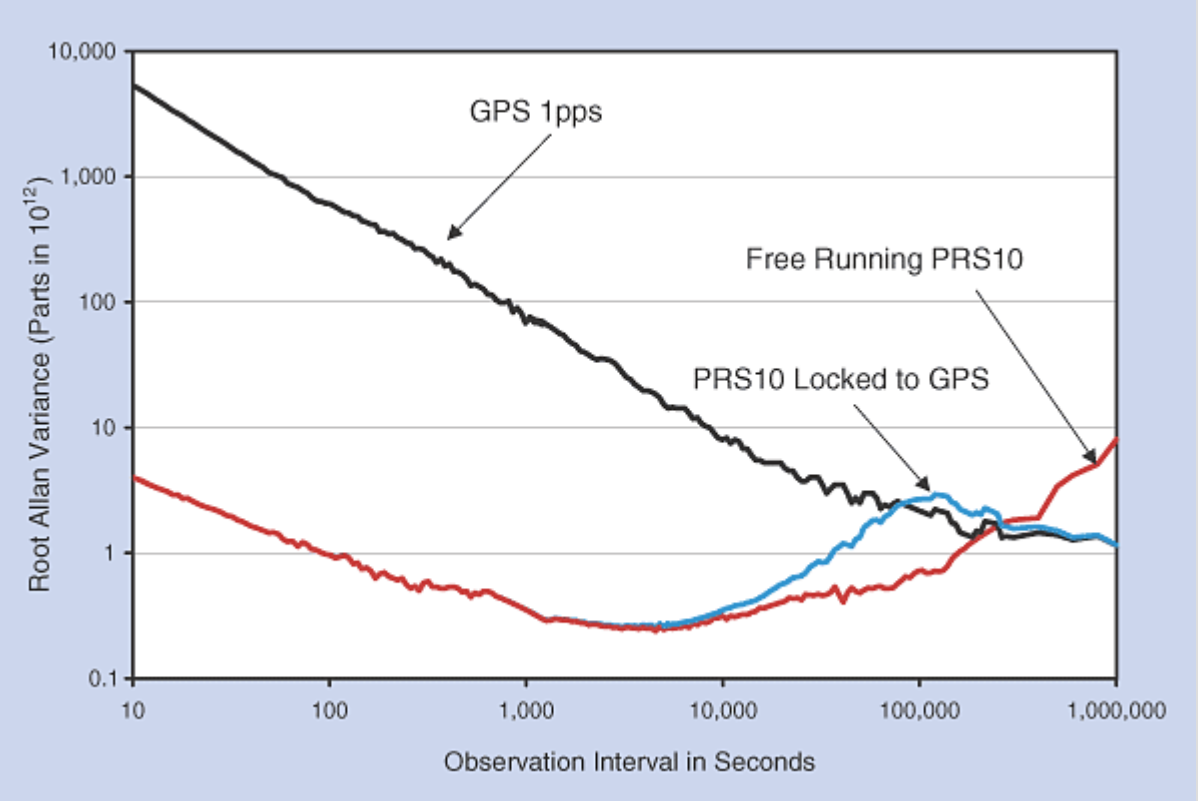
- 122.88 MHz clock to drive RF modules
- Pulse-per-second and timestamps for data tagging
- 10 MHz general purpose reference signal
- Total Electron Count observation/reporting
- Specifications (as declared by the team):
  - Frequency accuracy (long-term): $<1x10^{-12}$
  - Frequency stability: $<1x10^{-9}$ (1 part per billion) at tau >= 1 second
  - PPS accuracy: within 100 nanoseconds of UTC(USNO)
  - PPS jitter: <10 nanoseconds
  - Phase noise (122.88 MHz):
    - -80 dBc/Hz @ 100 Hz offset
    - -150dBc/Hz @ 100 kHz offset

GPSDO Theory

- GPS has long-term accuracy and stability, but noisy in the short term; crystal oscillator has short-term stability but drifts and is environmentally sensitive.
- Use phase-lock loop with suitable time constant to steer crystal to stay lined up with GPS



The GPSDO Visualized

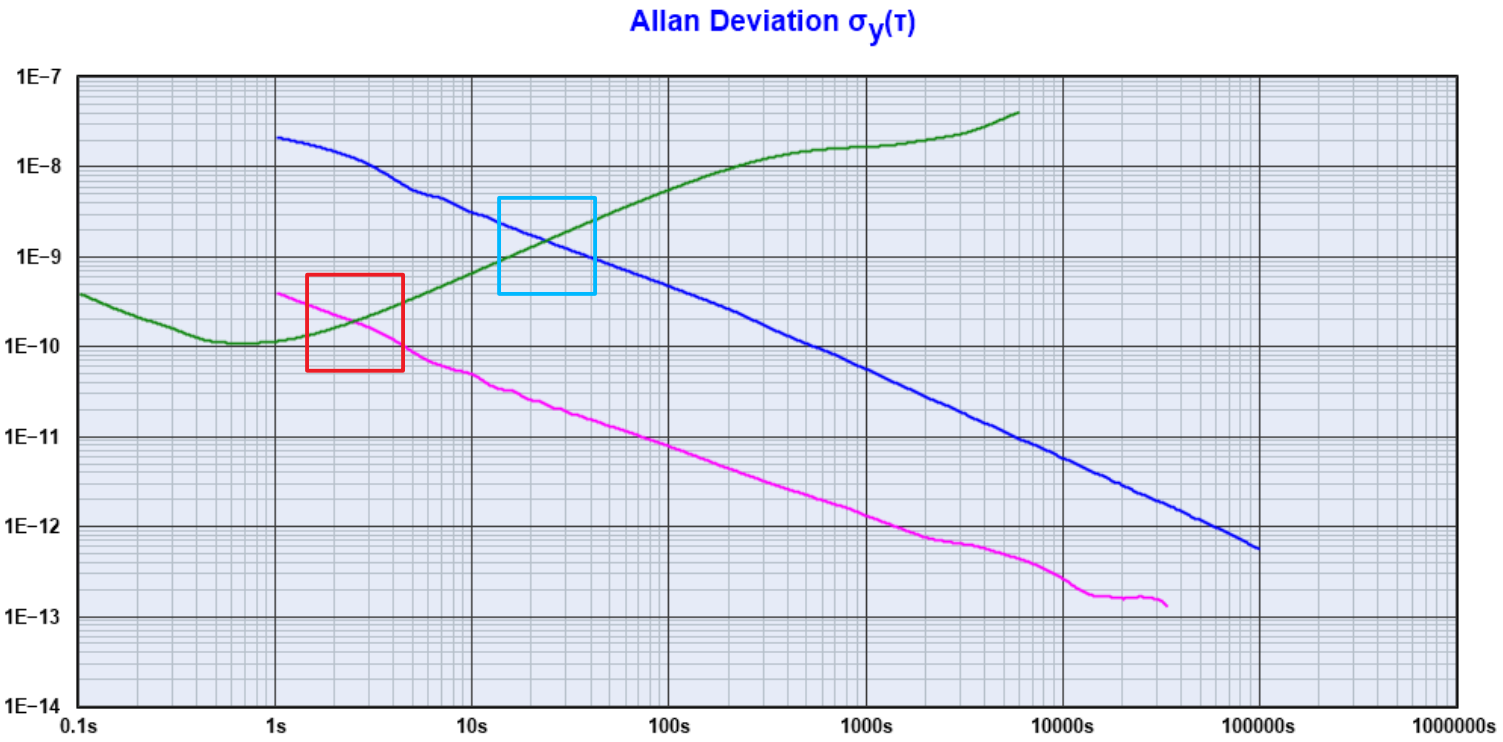


Source: https://www.thinksrs.com/products/prs10.htm

Taking Advantage of GPS Performance Improvements

- Dual-Frequency GPS (e.g., ZED-F9T) provides ½ order of magnitude improvement
- Sawtooth correction provides a full order of magnitude
- Net result is short term PPS noise of around 5×10^{-10}
  - That actually ***exceeds*** our short-term specification!
- This low jitter allows a PLL with a time constant of a few seconds, rather than a few hundred
  - And that reduces the performance requirements for the local oscillator
- The ADEV plot tells the tale...

The Magic Plot



Trace	Notes	Sample Interval	Acquired	Instrument
Sparkfun EM-406A (SiRF III)	TVB Maser	1 s	400000 pts	HP 53132A
ZED-F9T Corrected PPS	vs HP 5071A	1 s	140000 pts	TICC
Vectron 125 MHz TCXO	vs HP 5071A	0.100 s	246082 pts	TICC

Key GPSDO Design Points

- Use low PPS noise to allow short PLL time constant
- Phase lock 122.88 MHz TCXO directly; no 10 MHz XO
  - 10 MHz output available via synthesis in FPGA
- FPGA serves as connection matrix and processor
- Lots of extra I/O to allow different implementations, *e.g.*:
  - Use 10 MHz XO for traditional design
  - Use low-noise synth chip to generate 122.88 MHz
  - Use external 10 MHz input as reference
- Module can be used independently of TangerineSDR
  - *e.g.*, adapter shield to mount on Raspberry Pi
- Hardware and firmware are Open Source

Clock Module Block Diagram