Harris Semiconductor

APPNOTE

Digital Signal Processing

Loading Custom Digital Filters Into the HSP50110/210EVAL

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Introduction

The HSP50110/210EVAL was intended to showcase the demodulation capabilities of the HSP50110 Digital Quadrature Tuner (DQT) and the HSP50210 Digital Costas Loop (DCL). This chipset was designed to handle primarily BPSK, QPSK, and OQPSK 10-bit sampled input waveforms data rates up to 52MHz. While many aspects of the chip are programmable, the filter coefficients are fixed. The filters provided within both chips will yield acceptable BER for most QPSK systems. However, if the system requires unique matched filtering or a nonstandard data convolution, then an additional digital filter must be placed either in front of the DQT, between the DQT and DCL, or after the DCL. Filtering before the DQT requires a digital filter to operate at rates greater than 52MHz (in order to ensure the convolution sum is completed every 19ns). Filtering after the DCL, which is after demodulation and symbol detection, allows aliasing and other corruption to pass through the downconversion into the baseband. Thus, the HSP50110/210EVAL platform provides for additional filtering between the DQT and DCL, where the aliasing and other corruptions can be removed prior to the baseband filtering and symbol detection at a reasonable processing rate.

The HSP50110/210EVAL provides the user the option of using a programmable HSP43124 Serial I/O filter for data shaping and frequency characterizing. This application note discusses how to program the serial filter using the SERINADE™ software development tool and the HSP50110/210EVAL configuration control software (demodevb.exe).

First, the paper discusses square root of raised cosine (RRC) filters, since the HSP50210 has an internal 15-tap α = 0.4 RRC filter. A prototype RRC filter impulse response will be created. This coefficient set will be used to demonstrate the process of programming the serial filter. Custom coefficient sets for other filter types can be loaded using the same steps detailed in this process.

Second, the coefficients are then stored in a text file. This file will have a special header attached to it so that SERINADE can import it.

Next, SERINADE will then be used to generate a report file and configure decimations rates between the DQT and DCL. Serinade parameters that need to be changed will be highlighted.

Finally, the RRC filter created in the first step and formatted in the second and third steps will actually be loaded into HSP50110/210 Evaluation Board.

Root-Raised Cosine Background Information

The square root raised cosine filter is derived from a broader class of filters called raised cosine filters. Raised cosine (RC) filters have zero crossings where the adjacent symbols are suppose to occur. Figure 1 is an example of a raised cosine filter. The center of the symbols are designated by the dotted lines. If the received signal contains a lot of intersymbol interference (ISI), the raised cosine filter suppresses the information from adjacent symbols. The adjacent information is zeroed out during the convolution.
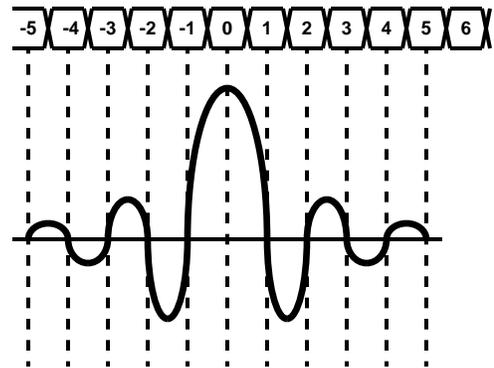
FIGURE 1. RRC FILTER CONVOLVING WITH A DATA SOURCE

Figure 2 shows some conceptual placements of the RC filter for a system with ISI. The third option uses two filters called root raised cosine (RRC) filters. The RRC filter has a frequency response equal to the square root of the frequency response of an RC filter. Remember that convolution in the time domain is equal to multiplication in the frequency domain. The data is convolved with the first RRC filter; the result is transmitted over a medium. The recovered data is again convolved an RRC filter. Thus the resulting frequency responses are equal to the original RC filter. Due to the one-to-one properties of transforms, equivalent frequency responses implies that the time domain responses are equivalent. The HSP50110/210 yields optimum BER performance when the transmitted data has been shaped by an RRC filter.
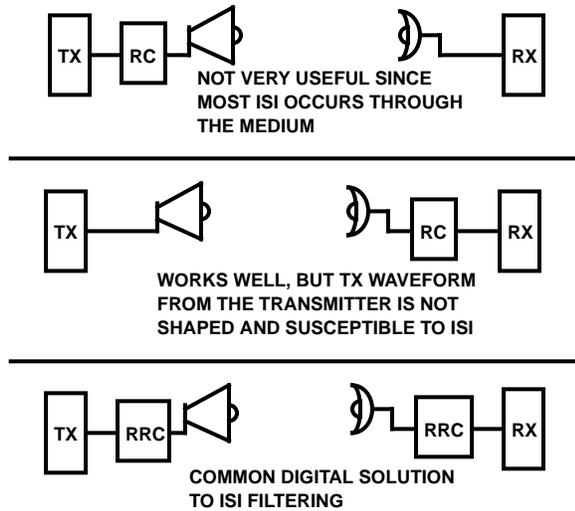
FIGURE 2. CONCEPTUAL ISI FILTERING; THE FILTERING WOULD OCCUR WITHIN THE TX AND RX SYSTEM

The general RRC filter impulse response can be defined as

$$h(t) = \frac{4\alpha}{\pi\sqrt{T}} \left[\frac{\cos\left((1+\alpha)\pi\frac{t}{T}\right) + \frac{\sin\left((1+\alpha)\pi\frac{t}{T}\right)}{4\alpha t/T}}{1 - (4\alpha t/T)^2} \right] \quad \text{(EQ. 1)}$$

where t is time index, T is how many times faster the filter is operating than the symbol rate, and α is the ratio of excess bandwidth past the 3dB point to the total bandwidth of the filter.

Lets examine an α = 0.2 2xSymbol Rate RRC filter case. The code in Figure 3 was developed using a popular commercial software tool and Equation 1. Sixteen taps were selected to enable the user to regenerate an identical filter as rrc2a2x.imp from the filters directory of the HSP50110/210 distribution disk. Figure 4 shows the resulting gain of 1 impulse response filter.

```
n=-7:8;  % n is an integer index from -7 to 8 in steps of 1.

alpha = 0.2, T = 2, delta= -.5;

n=n+delta+.0001;  % creates proper offset in index for cases

% where intersymbol interference attenuation is needed.

scale = 4*alpha/(pi*sqrt(T));

A = cos((1+alpha)*pi*n/T);

B = sin((1-alpha)*pi*n/T)./(4*alpha*n/T);

C = 1-(4*alpha*n/T).^2;

h = scale*(A+B)./C;

h=h/sum(h);  % sets the filter gain to 1
```

FIGURE 3. PSEUDO-CODE USED TO GENERATE AN RRC FILTER
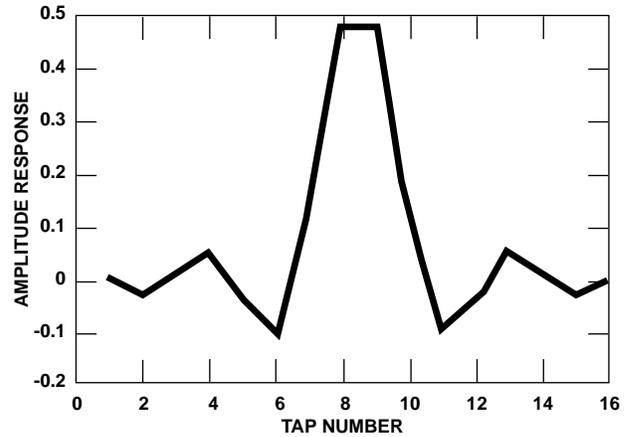
FIGURE 4. IMPULSE RESPONSE OF THE 16 TAP RRC FILTER CREATED

Figure 5 shows the frequency response of the 16 tap filter convolved with itself. Recall that this frequency response is equal to the frequency response of the system's raised cosine filter. Note that α approximately equals (79-61)/61 = 0.295. By limiting the number of taps to 16, the IIR filter response given in Equation 1 is in effect, windowing. This windowing will result in the frequency response of the original IIR filter being convolved with a sin(x)/x function. The lower number of taps, the bigger the ripples in the passband due to the sin(x)/x frequency response of the smaller window. So with 16 taps, the α can only be approximated, and ripples exist in the passband.
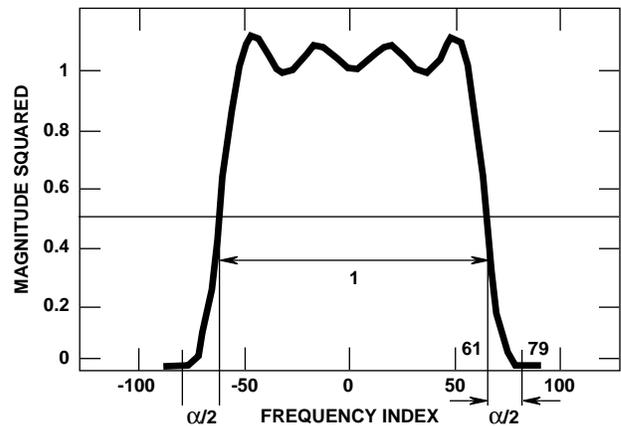
FIGURE 5. 256 POINT FFT OF THE 16 TAP RRC FILTER CONVOLVED WITH ITSELF

The frequency response of the raised-cosine filter is the main concern, since the RRC on the transmit side is convolved with the RRC on the received side. Together, they provide the intersymbol interference suppression required. A theoretical frequency response of an RC filter is given in Figure 6.

The RRC filter in Figure 6 was created with the same code used to generate the 16 tap filter. The index went from -127 to 128 instead of -7 to 8. This filter is essentially a 256 tap version of the previous filter. The greater the number of taps, the closer measured α reaches the theoretical.
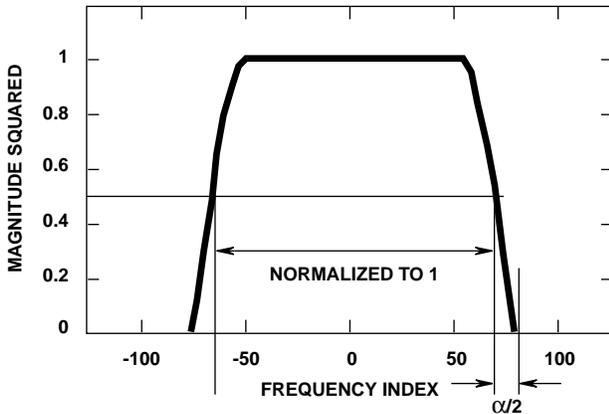
FIGURE 6. FREQUENCY RESPONSE OF AN IDEAL RRC

In our example we used a 2xbaud RRC filter. If we are running at a sampling frequency Fs that is 2 times faster than baud, then the filter cut off frequency should be half the sampling frequency, or Fs/2, which is equal to the baud rate. There is no reason why the filter can not run at Nx baud, making -Fs/N to Fs/N the filter passband.

To compute α, always normalize the frequency ranges so that the range -Fs/N to Fs/N equals one. As shown in our 256 tap α = 0.2 2x RRC filter on the previous slide, α can be verified using the RC frequency response by measuring the bandwidth between the 3dB point (= 0.5 on the linear scale) down to the zero magnitude point. α is obtained by dividing this measurement by Fs/N. As seen in the previous examples, the practical value of these calculations may or may not exactly matched the theoretical α used in Equation 1 to generate the impulse response.

An additional characteristic of RRC filters is that mismatched RRC α's will have minimal effect on bit error rate tests. The mismatch acts similar to a noise source of relative amplitude shown in Figure 7 also add the mismatch filter reference. All mismatches have at least -28dB of degradation which translates into a negligible addition to the probility of error on the BER curve. Thus, for typical α values between 0.3 and 0.7, there is no need to use a RRC custom filter.
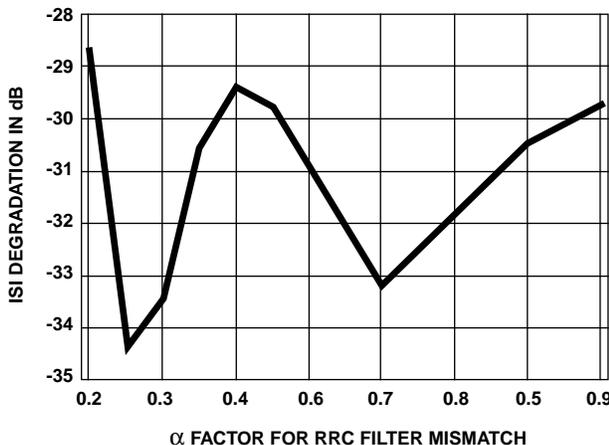
FIGURE 7. EFFECTS OF α MISMATCH TO THE α = 0.4 RRC FILTER ON THE HSP50110/210EVAL

Modifying Custom Filter Impulse Responses For SERINADE

In our commercial software package, we saved our filter file coefficients as a text file. To this text file, a 7 line header needs to be added in order for SERINADE to read it. The first six lines are not really read by SERINADE; however users should take advantage of this space to define the filters verbally. The 7th line requires an "r 1 16", where r tells SERINADE that the text file is a real data set, 1 tells SERINADE to read one column, and 16 tells SERINADE that 16 lines of data should be read. For an M-tap filter, an M should be used instead of 16. The modified file needs to have the "*.imp" suffix attached to the desired file name. The SERINADE software assumes this suffix is a text file of the format describe in column 2 of Figure 8.

SAVED TEXT FILE	SERINADE "_.IMP" FILE
	"rrc2a2x.imp"
	Root Raised Cosine Filter Coefficient File
	Alpha = 0.20
	Tap Spacing = 0.5-0.001 Baud
	D.C. Gain = 1
	Maximum Output = 1.682
	r 1 16
0.0000	0.0000
-0.0296	-0.0296
0.0108	0.0108
0.0529	0.0529
-0.0367	-0.0367
-0.1018	-0.1018
0.1284	0.1284
0.4760	0.4760
0.4760	0.4760
0.1283	0.1283
-0.1018	-0.1018
-0.0367	-0.0367
0.0529	0.0529
0.0108	0.0108
-0.0296	-0.0296
0.0000	0.0000

FIGURE 8. TEXT TO SERINADE FILE CONVERSION

Using SERINADE to Import Custom Filter Responses

This section will detail how to import the modified text file created in the previous section into SERINADE. The SERINADE parameters that need to be changed will be highlighted and a SERINADE report file will be created. Assume that the name of our file modified text file is "rrc2a2x.imp". Figures 9 and 10 have each parameter that is changed highlighted with the step number from the following instructions:

1) Set FIR type to IMPORTED by toggling with space bar.

2) Select filter path and name. The impulse response filter "rrc2a2x.imp" is located in the C: drive in the customer\field subdirectory of our PC. Users may place there *.imp files elsewhere.

3) Note that these values don't really mean anything. In the display, these are used to draw the nice green lines which really do not mean anything. The filter is set by the impulse response in rrc2a2x.imp.

4) If a Decimation error flashes on the screen, make sure to set the FIR decimation and the Halband filter decimation to the desired configuration.If the input of the DCL is equal to the output of the DQT, the FIR decimation should be set to 1 and Halfband order to 0.

5) Set Serinade up to save RPT file. Add filter name and path that is custom to current configuration.

```
+--------------------------------------------------------------+
|                                                              |
|          |F1 - Help   F2 - Start Design   F3 - Save File   F10 - Exit|
+--------------------------------------------------------------+
+-----+       HSP43124 SERIAL I/O FILTER SPECIFICATION
|    |
| S | Filter File      : c:\customer\field\rrc2a2x.SER
|    | Input Sample Rate: 2.36000   MHz       Design Mode      : MANUAL
| E | Decimation Factor: 1                    Generate Report  : YES
|    | Passband       : 590.00000  kHz        Display Response : LOG
| R | Transition Band  : 150.00000 kHz  Save Freq Responses : YES
|    | Passband Atten  : 1.50000     dB
| I | Stopband Atten  : 14.70474    dB       FIR Order         : 16
|    | Input Bits      : 16
| N | Output Bits     : 16                    FIR Decimation    : 1
|    | FCLK          : 38.94000  MHz      HB Order          : 0
| A | FIR Type      : IMPORTED           FIR Symmetry     : EVEN
|    | FIR File        : c:\customer\field\rrc2a2x.IMP
| D |
|    |            HSP43124 CONFIGURATION
| E | Output Data Rate : 2.36000   MHz       HB Decimation     : 1
|    | Max FCLKS/CLKOUT : 1
|    | Min SCLK        : 37.76000   MHz
|    | Min FCLK        : 21.24000   MHz
|    |
+----+
```

FIGURE 9. STEPS 1, 2 AND 3 FOR THE SERINADE USER'S SCREEN

```
+--------------------------------------------------------------+
|          |F1 - Help   F2 - Start Design   F3 - Save File   F10 - Exit|
+--------------------------------------------------------------+
+-----+       HSP43124 SERIAL I/O FILTER SPECIFICATION
|    |
S | Filter File      : c:\customer\field\rrc2a2x.SER
| Input Sample Rate: 2.36000   MHz       Design Mode      : MANUAL
E | Decimation Factor: 1                    Generate Report  : YES
| Passband       : 590.00000  kHz        Display Response : LOG
R | Transition Band  : 150.00000 kHz   Save Freq Responses: YES
| Passband Atten  : 1.50000     dB
I | Stopband Atten  : 14.70474    dB       FIR Order         : 16
| Input Bits      : 16
N | Output Bits     : 16                    FIR Decimation    : 1
| FCLK          : 38.94000  MHz      HB Order          : 0
A | FIR Type      : IMPORTED           FIR Symmetry     : EVEN
| FIR File        : c:\customer\field\rrc2a2x.IMP
D |
|            HSP43124 CONFIGURATION
E | Output Data Rate : 2.36000   MHz       HB Decimation     : 1
| Max FCLKS/CLKOUT : 1
| Min SCLK        : 37.76000   MHz
| Min FCLK        : 21.24000   MHz
|
+----+
```

FIGURE 10. STEPS 4 AND 5 FOR THE SERINADE USER'S SCREEN

Hit F2, and the SERINADE software creates the proper filter report filer. Figure 11 shows the frequency response that is displayed on the screen.

SYSTEM FREQUENCY RESPONSE
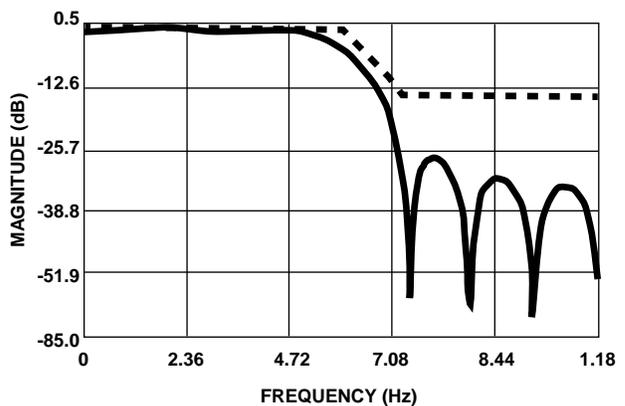
FIGURE 11. FREQUENCY PLOT GENERATED BY SERINADE

A copy of SERINADE can be obtained from the Harris Semiconductor web site located at http://www.semi.harris.com. Select the DSP Products button. From the DSP Standard Product page, select the Product Development tools. Select the SERINADE software tools and download the needed files. Once loaded, run "serinade.exe" from either windows or from the DOS prompt. The report file created by SERINADE is stored as a *.RPT file. This file is used by the HSP50110/210EVAL kit's software to program the on-board HSP43124.

Loading RPT Files into the HSP50110/210 Evaluation Board

The HSP50110/210EVAL kit includes a distribution disk so that users can easily program the evaluation board. The executable that should be run is called "demodevb.exe". When software demodevb.exe is executed, the menu shown in Figure 12 appears.

```
+-----------------------------------------------------------+

    HSP50110/210 EVALUATION BOARD SOFTWARE

+-----------------------------------------------------------+
                      MAIN MENU
      (1) Data Path/Modulation Setup
      (2) Carrier Tracking Loop Setup
      (3) Bit Sync Loop Setup
      (4) Acquisition and Tracking Setup
      (5) Load Configuration File
      (6) Save Configuration File
      (7) Generate Output Files
      (8) Configure Hardware
      (9) Exit
      ENTER SELECTION:
```

FIGURE 12. MAIN MENU FOR THE HSP50110/210EVAL SOFTWARE

The following steps detail loading the HSP50110/210 with the *.RPT report file created by SERINADE. The rrc2a2x.rpt file will be used as the file. When a custom file has been generated, that report file's name should be used instead.

Enter a '1' to select the Data Path/Modulation setup. The menu appears as shown in Figure 13.

```
+-----------------------------------------------------------------+

      HSP50110/210 EVALUATION BOARD SOFTWARE

+-----------------------------------------------------------------+

              DATA PATH / MODULATION MENU
   Current File Name.. .\EXAMPLES\Q1024RRC

(1) Master Clock Freq.. 40000000 Hz  (15) Es/No (min).........  +0     dB
(2) Input Sample Rate.. 40000000 Hz  (16) Es/No (max)......... +100   dB
(3) Input Mode......... Gated        (17) Es/No (design)......  +4     dB
(4) DQT Input Samples.. Real         (18) A/D backoff (min)...  12     dB
(5) DQT Input Format... Offset Bin.  (19) A/D backoff (max)...  18     dB
(6) L.O. Center Freq... +5000000 Hz  (20) DCL Output Vector...  -6     dBFS
(7) Data Modulation.... BPSK         (21) DQT Output Level.... -12    dBFS
(8) Baud Rate.......... 128000   Hz  (22) DCL Detect. Level... -12    dBFS
(9) DQT Output Rate.... 256000 Hz    (23) Slicer Threshold.... 0.25
(10) I.F. NBW........... 6000000 Hz  (24) DQT AGC Slew Rate...20   dB/sec
(11) DQT Filter......... CIC w/ comp (25) DCL AGC Slew Rate... 5   dB/sec
(12) DCL RRC Filter..... Enabled     (26) AGC Limits:......... Full Range
(13) DCL I&D........... Bypassed     (27) Output Mux Select... 7
(14) HSP43124 .......... Bypassed
 (0) Main Menu
ENTER SELECTION:
          (C) Harris Semiconductor 1996 Version 1.01
```

FIGURE 13. DATA PATH/MODULATION MENU

Enter a 12 and disable DCL RRC Filter. The software will revert to the Data Path/Modulation menu. Notice item 12 has changed from "Enabled" to "Bypassed" as shown in Figure 14.

```
+--------------------------------------------------------------------------+
|                                                                          |
|     HSP50110/210 EVALUATION BOARD SOFTWARE                               |
|                                                                          |
+--------------------------------------------------------------------------+
| DATA PATH / MODULATION MENU                                              |
|   Current File Name.. .\EXAMPLES\Q1024RRC                                |
| (1) Master Clock Freq.. 40000000 Hz   (15) Es/No (min)......... +0    dB |
| (2) Input Sample Rate.. 40000000 Hz   (16) Es/No (max)......... +100  dB |
| (3) Input Mode......... Gated         (17) Es/No (design)...... +4    dB |
| (4) DQT Input Samples.. Real          (18) A/D backoff (min)... 12    dB |
| (5) DQT Input Format... Offset Bin.   (19) A/D backoff (max)... 18    dB |
| (6) L.O. Center Freq... +5000000 Hz   (20) DCL Output Vector... -6   dBFS|
| (7) Data Modulation.... BPSK          (21) DQT Output Level.... -12  dBFS|
| (8) Baud Rate.......... 128000 Hz     (22) DCL Detect. Level... -12  dBFS|
| (9) DQT Output Rate.... 256000 Hz     (23) Slicer Threshold.... 0.25     |
| (10) I.F. NBW........... 6000000 Hz   (24) DQT AGC Slew Rate...20 dB/sec |
| (11) DQT Filter......... CIC w/ comp  (25) DCL AGC Slew Rate... 5 dB/sec |
| (12) DCL RRC Filter..... Bypassed     (26) AGC Limits:......... Full Range|
| (13) DCL I&D........... Bypassed      (27) Output Mux Select... 7        |
| (14) HSP43124 .......... Bypassed                                        |
| (0) Main Menu                                                            |
| ENTER SELECTION:                                                         |
|          (C) Harris Semiconductor 1996 Version 1.01                      |
+--------------------------------------------------------------------------+
```

FIGURE 14. DATA PATH/MOD MENU MODIFIED IN ITEM 12

```
+--------------------------------------------------------------------------+
|                                                                          |
|     HSP50110/210 EVALUATION BOARD SOFTWARE                               |
|                                                                          |
+--------------------------------------------------------------------------+
|                     DATA PATH / MODULATION MENU                          |
|   Current File Name.. .\EXAMPLES\Q1024RRC                                |
| (1) Master Clock Freq.. 40000000 Hz  (15) Es/No (min)......... +0    dB  |
| (2) Input Sample Rate.. 40000000 Hz  (16) Es/No (max)......... +100  dB  |
| (3) Input Mode......... Gated        (17) Es/No (design)...... +4    dB  |
| (4) DQT Input Samples.. Real         (18) A/D backoff (min)... 12    dB  |
| (5) DQT Input Format... Offset Bin.  (19) A/D backoff (max)... 18    dB  |
| (6) L.O. Center Freq... +5000000 Hz  (20) DCL Output Vector... -6   dBFS |
| (7) Data Modulation.... BPSK         (21) DQT Output Level.... -12  dBFS |
| (8) Baud Rate......... 128000    Hz  (22) DCL Detect. Level... -12  dBFS |
| (9) DQT Output Rate.... 256000 Hz    (23) Slicer Threshold.... 0.25      |
| (10) I.F. NBW........... 6000000 Hz  (24) DQT AGC Slew Rate...20  dB/sec |
| (11) DQT Filter......... CIC w/ comp (25) DCL AGC Slew Rate...5   dB/sec |
| (12) DCL RRC Filter..... Bypassed    (26) AGC Limits:......... Full Range|
| (13) DCL I&D........... Bypassed      (27) Output Mux Select... 7        |
| (14) HSP43124 .......... .\filters\rrc2a2x                               |
| (0) Main Menu                                                            |
| ENTER SELECTION:                                                         |
|          (C) Harris Semiconductor 1996 Version 1.01                      |
+--------------------------------------------------------------------------+
```

FIGURE 16. DATA PATH/MOD MENU MODIFIED IN ITEM 14

Enter 14 at the Data Path/Mod Menu. The first four lines of Figure 15 will appear. Enable HSP43124, and the program will ask for a file name to be entered. If a name is not entered, the prefix listed in the "Current File Prefix" is used as the default. Note that in the "filters" directory is one directory below where the demodevb.exe is being operated. Thus the specific data path must precede the file name in order for the program to find the report file.

```
+--------------------------------------------------------------+
|                                                              |
| Current Value: 0                                             |
|                                                              |
|    0 = HSP43124 filters bypassed                             |
|                                                              |
|    1 = HSP43124 filters enabled                              |
|                                                              |
|    Enter New Value [0]: 1                                    |
|                                                              |
|    Current File Prefix:  rrc8xa5                             |
|                                                              |
|    Enter File Prefix (.RPT exten. assumed):  .\filters\rrc2a2x|
|                                                              |
+--------------------------------------------------------------+
```

FIGURE 15. THE SUBMENU FOR ITEM 14 OF THE DATA PATH/MOD MENU

The filter name is the rrc2a2x.rpt without the rpt extension. The program will automatically look for the file name with the *.rpt suffix.

The program, after recording this change, will return to the Data Path/Mod Menu as shown in Figure 16. Note that item 14 has changed.

Enter 0 and return to the main menu in Figure 12.

In the Main Menu, enter 7 to generate the proper output files. If the wrong path to the rrc2a2x.rpt file was entered for item 14 of the Data Path/Mod menu, the program will notify you and kick back into the Main Menu. If this occurs, go back to the Data Path/Mod Menu and correct item 14.

Otherwise, the program will process all the files and load the microcontroller. When the processing is complete, it will return you to the main menu. Hit 8 and do a full initialization. The HSP50110/210 should now be operating with a rrc2a2x filter.

The RRC filter in item 12 was disabled before implementing the rrc2a2x. Some applications may actually have a need for both matched filter and RRC filter. If the RRC filter internal to the HSP50210 is sufficient, then the match filtered should be loaded into the HSP43124, and item 12 should be enabled. If a different RRC filter is required, then the RRC coefficients should be convolved with the matched filter coefficients. The resulting filter should be loaded into the HSP43124, and item 12 should be disabled.

Summary

Two topics were covered in this application note that will help users of the HSP50110/210EVAL. For those unfamiliar with root-raised cosine filters, the fundamentals of RRC filters were discussed. The second topic covered the loading of custom filter coefficients into the HSP43124 Serial I/O filters. An example RRC filter was used to demonstrate the total process of loading custom coefficients.